Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DAVID A. KAYSEN

Appeal No. 2003-0553
Application No. 09/137,285

ON BRIEF

Before FLEMING, BARRY, and LEVY, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-20. The appellant appeals therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue on appeal connects a peripheral to a computer system. A computer system uses a processor and a memory to control the operation of peripherals connected to the computer system via a bus. (Spec. at 1.)

In some computer systems, peripheral devices must meet certain requirements to operate correctly. For example, explains the appellant, peripherals must have adequate power and cooling to operate with an "enhanced computer system." Peripherals without such capabilities can impede the operation of the entire system. (*Id.*)

Accordingly, the appellant's invention controls whether a particular peripheral may be connected to a particular computer system. Based on the needs of a particular computer system, codes may be provided to authorized vendors of peripherals; peripherals meeting standards and specifications are provided with such a code. When a user connects a peripheral to a computer system, the code is sent from the former to the latter. The computer system checks the code to determine whether the peripheral is an authorized peripheral. If so, communications are allowed. If not, communications are prevented, and the user is notified that the peripheral cannot be used with the computer system. (*Id.* at 12.)

A further understanding of the invention can be achieved by reading the following claim.

> 1. A link for connecting a computer system, including a processor, with a peripheral comprising:
>
> a first connector that couples to said system;

a second connector that couples to said peripheral;

a first device that checks a code received through said first connector from said second connector;

a second device that provides a code to said first device through said first and second connector; and

said first device controlling communication between said computer system and said peripheral based on said code.

Claims 1-20 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,202,997 ("Arato").

OPINION

Our opinion addresses the claims in the following order:

- claims 1-8
- claims 9-20.

A. CLAIMS 1-8

Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the point of contention therebetween. The examiner makes the following assertions.

As per claims 1, 9, 12 and 15, and 18, Arato teaches a link for connecting a computer system (see Fig. 1-3), comprising a first connector that connects to said system (see ref col. 3 lines 4 et seq); and a second connector that connects to said peripheral (see ref col. 3 lines 4 et seq) ; a

> first device that controls communication between said computer system and peripheral based on a code (see ref col. 4 lines 5 et seq of the specification et seq), a first device that checks code received through a first connector and a second device that provides a code to the first device (see ref fig 1-3, col. 4 lines 16 et seq), a processor (fig 1 element 10), a storage device (fig 1 element 12), an interface (see ref fig 1-3 element 18).

(Examiner's Answer at 3.) The appellant argues, "there is no teaching in Arato of a second device that provides a code to enable a controlled communication between the peripheral and the computer system based on the code," (Appeal Br. at 6), and "there is no second device at the peripheral itself." (*Id*.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claim at issue to determine its scope. Second, we determine whether the construed claim is anticipated.

1. Claim Construction

"Analysis begins with a key legal question -- *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000).

Here, claim 1 recites in pertinent part the following limitations: "[a] link for connecting a computer system, including a processor, with a peripheral comprising: a first connector that couples to said system; a second connector that couples to said peripheral; a first device that checks a code received through said first connector from said second connector; a second device that provides a code to said first device through said first and second connector. . . ." Giving the claim its broadest, reasonable construction, the limitations require a link between a computer system and a peripheral, the link including a first device connected to a second device via a fist connector and a second connector, wherein the second device is coupled to a peripheral and provides a code to the first device and the first device checks the code.

2. Anticipation Determination

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220

USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, Arato discloses "a computer system incorporating an access control module. . . ." Col. 2, ll. 55-56. The "computer system compris[es] a CPU 10, internal memory 12, and two peripherals, a printer 14 and a disk drive 16." Col. 3, ll. 4-6. An I/O channel links the CPU, internal memory, and peripherals. Specifically, "[t]he CPU 10 communicates with the two peripherals via an I/O channel 18 having address lines 20 which conduct peripheral address signals, control lines 22 which conduct inter alia address validation signals, and a data bus 24 which serves to transfer data between the CPU 10 and the peripherals during read and write operations. The I/O channel 18 is constituted by a general purpose data bus whose various lines 20, 22, 24 are also used to address memory locations in the internal memory 12 when the data bus is not being used in connection with peripheral I/O operations." Col. 3, ll. 7-17. Furthermore, "[a]n access control module (ACM) 26 is attached to the I/O channel 18 in much the same manner as are the peripherals 14, 16." *Id.* at ll. 50-52.

"[E]ach peripheral might typically have an interfacing board commonly referred to as a 'card' which is mounted in a receptacle commonly referred to as a 'slot'." *Id.* at ll. 53-56. The "computer . . . might typically have in its interior a number of such slots so that various peripherals can be conveniently added to the system. For such systems, the ACM 26 is preferably formed on a card which can be inserted directly into a vacant slot, permitting very convenient connection to the system I/O channel." *Id.* at ll. 56-62.

We are uncertain on which components of the reference that examiner reads the claimed first connector, second connector, first device, and second device. The examiner appears to read both the first connector and the second connector on the same column of Arato, without referring to specific components mentioned therein. (Examiner's Answer at 3.) Similarly, he appears to read both the first device and the second device on the same lines and column of the reference, without referring to specific components mentioned therein. (*Id.*) We will not "resort to speculation," *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), as to the examiner's position. Therefore, we reverse the rejection of claims 1-8.

B. CLAIMS 9-20

The examiner asserts, "the concept of having a code to establish or control communication between a peripheral and a computer system is inherent in Arato . . . because computer system usually has code set in their memory from the manufacture that enables them to communicate with certain peripherals." (Examiner's Answer at 3.) The appellant argues, "nowhere in the Arato reference the Appellant finds that the peripheral provides the code to identify itself, as claimed in claim 18. Rather, according to the Arato reference, the CPU 10 generates the address signal, which uniquely identifies the selected peripheral. See col. 3, lines 23-31, and col. 4, lines 5-7." (Reply Br. at 2.)

1. Claim Construction

Independent claim 9 recites in pertinent part the following limitations: "determine whether a code received from said peripheral corresponds to a code identifying the peripheral as one that may be used with the computer system;" independent claim 18 includes similar limitations. Similarly, independent claim 12 recites in pertinent part the following limitations: "causing a peripheral to provide a code to a computer system which identifies said peripheral;" independent claim 15 includes similar limitations. Giving claims 9, 12, 15, and 18 their broadest, reasonable construction, the limitations require that a peripheral generate and send a code identifying itself to a computer.

2. Anticipation Determination

In Arato, an "address signal, propagated along the address lines 20 . . . uniquely identifies [a] selected peripheral." Col. 3, ll. 24-27. We are unpersuaded, however, that the reference's peripherals generate or send such address signals. To the contrary, the first passage cited by the appellant discloses that "the CPU 10 . . . generate[s] [the] address signal, propagated along the address lines 20, which uniquely identifies the selected peripheral." Col. 3, ll. 25-27. The second passage cited by the appellant further disclose that "the ACM 26 responds to and acts on each valid address signal **generated by the CPU**." Col. 4, ll. 6-7 (emphasis added).

The absence of a peripheral generating and sending a code identifying itself to a computer negates anticipation. Therefore, we reverse the rejection of claim 9; of claims 10 and 11, which depend therefrom; of claim 12; of claims 13 and 14, which depend therefrom; of claim 15; of claims 16 and 17, which depend therefrom; of claim 18; and of claims 19 and 20, which depend therefrom.

CONCLUSION

In summary, the rejection of claims 1-20 under § 102(b) is reversed.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)
LANCE LEONARD BARRY Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)

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